**Abstract—**Reconfigurable SoC interconnected by an NoC architecture mandates a low power and small footprint reconfiguration scheme that enables multiple applications to effectively share precious hardware resources. The trade-offs between the static compilation and the dynamic reconfiguration has yet to be evaluated at the highest possible abstraction level of the NoC designs. In this paper, reconfiguration is thus considered during the application scheduling and mapping stage. That is, for a given set of applications which target to run on a dynamically reconfigurable NoC architecture, a schedule and map of these applications needs to be found to minimize the communication cost, while satisfying the timing, area and other applicable design constraints. The proposed solution follows a three-step design flow. In the first task scheduling step, multiple applications are scheduled to a minimal number of processor nodes while meeting the timing constraints. Next, applications that shall be mapped onto the same hardware resource but run at the different time instances through hardware reconfiguration are merged. In this step, effort is dedicated to minimize the reconfiguration cost. In the last step, all the applications are finally mapped onto the targeted NoC architecture. The experiment results have shown that the proposed method has achieved 50% area reduction than a conventional scheme that does not consider reconfiguration cost.

**Keywords—**NoC, Mapping, scheduling, reconfiguretion